WHAT IS CLAIMED IS:

1. A wireless peak suppression, phase and amplitude equalizer circuit for use with multi-carrier power amplifiers in a wireless communication system to enhance the linearity and performance of the amplifier, in particular wireless cellular, PCS, wireless LAN, line of sight microwave, military, and satellite communication systems and any other none wireless applications, the peak suppression, phase and amplitude equalizer circuit comprising:

   - A multi-carrier receiver for the peak suppression, phase and amplitude equalization of IF or RF input signal to amplifier. If the input signal is baseband then the multi-carrier receiver is bypassed.

   - A digital signal processing block to reduce peak-to-average of the multi-carrier input signal using amplitude clipping and phase rotation.

   - A digital signal processing block to use the amplitude clipped multi-carrier baseband signal to produce the phase rotation lookup table.

   - A digital signal processing block to converts the multi-carrier baseband input signal to individual carrier baseband signals. The individual carrier baseband signal is phase rotated before being up converted to its original multi-carrier baseband signal.

   - A digital signal processing block to phase equalize the individual carrier baseband signal after being amplitude clipped, phase rotated and filtered.

   - A digital signal processing block to amplitude equalize the individual carrier baseband signal after being amplitude clipped, phase rotated and filtered.

- A digital signal processing block to up converter the individual carrier to their original baseband frequency after being amplitude clipped, phase rotated, filtered, phase equalized, and amplitude equalized.

- A digital signal processing block that clips the amplitude of the multi-carrier baseband signal by preserving the phase.

- A multi-carrier transmitter block that prepares the peak-to-average reduced multi-carrier signal for delivery to multi-carrier power amplifier.

2. The peak suppression, phase and amplitude equalizer circuit according to claim 1, wherein main multi-carrier input signal from the wireless transmitter is sampled using sub-harmonic sampling technique at the input frequency or at an intermediate frequency.

3. The peak suppression, phase and amplitude equalizer circuit according to claim 1, wherein the multi-carrier input signal from the wireless transmitter is sampled using sub-harmonic sampling technique at the input frequency or at an intermediate frequency and the digitized multi-carrier input signal is decimated to the appropriate number of samples per symbol for further digital signal processing.

4. The peak suppression, phase and amplitude equalizer circuit according to claim 1, wherein the multi-carrier input signal from the wireless transmitter is baseband and is sampled using Nyquist sampling technique and interpolated to produce the baseband multi-carrier signal with appropriate number of samples per symbol.

5. The peak suppression, phase and amplitude equalizer circuit according to claim 1, wherein the multi-carrier input signals from the wireless transmitter are in bit domain and the bit domain baseband signals are up converted,

combined and interpolated to produce the digital multi-carrier baseband signal with appropriate number of sample per symbol.

6. The peak suppression, phase and amplitude equalizer according to claim 1, wherein the digital multi-carrier baseband signal is amplitude clipped without disturbing the phase before being down converted to produce individual carrier baseband representatives.

7. The peak suppression, phase and amplitude equalizer according to claim 1, wherein the amplitude clipped digital multi-carrier baseband signal is converted to single channel baseband signals by digital down conversion. The individual baseband signals are phase rotated using the phase from phase rotation lookup table, then filtered to eliminate the unwanted signals.

8. The peak suppression, phase and amplitude equalizer according to claim 1, wherein the individual carrier baseband signals after being phase rotated and filtered are phase equalized to maintain the phase property of the baseband signal before it was down converted.

9. The peak suppression, phase and amplitude equalizer according to claim 1, wherein the individual carrier baseband signals after being phase rotated, filtered, and phase equalized are amplitude equalized to maintain the modulation properties of the baseband signal before it was down converted.

10. The peak suppression, phase and amplitude equalizer according to claim 1, wherein the individual carrier baseband signals after being phase rotated, filtered, phase and amplitude equalized are up converted to their original baseband multi-carrier baseband frequency.

11. The peak suppression, phase and amplitude equalizer circuit according to claim 1, wherein the peak-to-average reduced signal is digitally up converted and converted to analog domain at an intermediate frequency or the output frequency.

12. The peak suppression, phase and amplitude equalizer circuit according to claim 1, wherein the peak-to-average reduced signal is converted to analog domain at baseband frequency and then up converted to IF or RF frequency in analog domain.

13. The peak suppression, phase and amplitude equalizer circuit according to claim 1, wherein the peak-to-average reduction phase rotation lookup table is created using the individual baseband representative of the amplitude clipped multi-carrier baseband signal and the amplitude clipped multi-carrier baseband signal.

14. The peak suppression, phase and amplitude equalizer circuit according to claim 1, wherein the received signal strength of the input signal to peak suppression, phase and amplitude equalizer circuit and transmit signal strength of the output from the peak suppression, phase and amplitude equalizer circuit is dynamically measures to adjust the total gain of the peak-to-average reduction circuit zero

15. The peak suppression, phase and amplitude equalizer circuit according to claim 1 and subsequent claims, when it is used in wireless cellular, wireless PCS, wireless LAN, microwave, wireless satellite, none wireless amplifiers, and any wireless communication systems used for military applications.

16. The peak suppression, phase and amplitude equalizer circuit according to claim 1, wherein the DSP function can be implemented in programmable logic, FPGA, Gate Array, ASIC, and DSP processor